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Realizing ternary quantum switching networks without ancilla bits

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Abstract

This paper investigates the synthesis of quantum networks built to realize ternary switching circuits in the absence of ancilla bits. The results we established are twofold. The first shows that ternary Swap, ternary NOT and ternary Toffoli gates are universal for the realization of arbitrary $n \times n$ ternary quantum switching networks without ancilla bits. The second result proves that all $n \times n$ quantum ternary networks can be generated by NOT, Controlled-NOT, Multiply-Two and Toffoli gates. Our approach is constructive.

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1. Introduction

Quantum computation connects ideas from computer science and physics [1]. Reversible circuits are a necessary subclass whose realization is required for any quantum computer to be universal. Three state quantum systems have recently been discussed in the framework of cryptography [2]³, and the concept of a qudit cluster state has been proposed [3]. Qudit systems received further study in [5] and [6] wherein quantum hybrid gates acting on the tensor products of qudits of different dimensions were discussed. Recently synthesis for d -level systems showing asymptotic optimality was also proposed [4]. The study in [5] and [7] found hybrid quantum gates that, when considered to be controlled by and act on three level quantum systems, define the hybrid Toffoli, Swap and NOT gates used in this paper. The physical realization of these hybrid gates might be accomplished via spin systems [5, 8] or quantum harmonic oscillators [5, 8]. A universal set of ternary quantum gates enables the realization of any tristate switching network on a candidate qudit realization.

³ Citations with 'quant-ph/xxxxxxx' designation are on the internet at <http://arxiv.org/http://arXiv.org/>.

The computer science community has also experienced recent interest in the universal sets of gates required for ternary quantum computing systems, the main results of which appear in [9–11]. In these gates, arbitrary Galois field operations are used in the so-called Toffoli gates of the ESOP-based (exclusive sums-of-products) realization of binary reversible circuits, where Galois addition and multiplication replace the XOR and AND gates, respectively. The ESOP circuit synthesis programs use heuristic rule-based search strategy to minimize each output as an exclusive sum-of-products realized as k -input ($k \leq n$) Toffoli gates. We observe that the universality discussed in the literature has an assumption that the inputs of gates can be set to constant values, thus ancilla bits are used [9–11]. These programs can be applied to large functions but their disadvantage is that they create m ancilla bits (one for each output) and use multi-input gates that may be expensive. Although [5] discussed entanglement generation⁴ with and without ancilla qudits, in both the physics and computer science communities neither the ternary switching universality of the introduced sets of gates nor the proof of a synthesis algorithms convergence was given.

Group theory [12] has found particular use to generate reversible logic circuits [13]. Some notable results appear in [13–16] which are applicable to the synthesis of quantum switching networks. The motivation of this paper is to find the universality of a gate family [17] to be used in synthesis of ternary reversible circuits without ancilla bits. We prove that ternary Swap, NOT and Toffoli gates [5] are universal for realization of arbitrary ternary $n \times n$ reversible circuits without ancilla bits. Moreover, we create an algorithm for one of these gate families that is provably convergent. Our algorithm is constructive and effective in both space and time resources.

This paper is organized as follows. First, in section 2, we introduce some basic definitions of ternary switching networks and the needed group theory notation, terms and results. We then present our main results: theorem 1 and 2 after four lemmas. Second, we conclude this paper. Finally, in the appendix, we prove lemma 4, and present two examples to illustrate the synthesis process for a given ternary reversible circuit.

2. Main results

This section begins by presenting some basic definitions of ternary switching networks and the needed group theory notation and terms.

Definition 1 (ternary reversible gate). *Let $B = \{0, 1, 2\}$. A ternary logic circuit f with n input variables, B_1, \dots, B_n , and n output variables, P_1, \dots, P_n , is denoted by $f : B^n \rightarrow B^n$, where $\langle B_1, \dots, B_n \rangle \in B^n$ is the input vector and $\langle P_1, \dots, P_n \rangle \in B^n$ is the output vector. There are 3^n different assignments for the input vectors. A ternary logic circuit f is reversible if it is a one-to-one and onto function (bijection). A ternary reversible logic circuit with n inputs and n outputs is also called an $n \times n$ ternary reversible gate. There are a total of $(3^n)!$ different $n \times n$ ternary reversible circuits.*

The concept of a permutation group and its relationship with reversible circuits will now be introduced.

Definition 2 (permutation). *Let $M = \{d_1, d_2, \dots, d_k\}$. A bijection⁵ of M onto itself is called a permutation on M . The set of all permutations on M forms a group under composition of*

⁴ The reader wishing to develop background in the theory of quantum computation should consult the textbook by Nielsen and Chuang [1] and the references therein.

⁵ Bijection: one-to-one, and onto mapping.

mappings, called a symmetric group on M . It is denoted by S_k [12]. A permutation group is simply a subgroup [12] of a symmetric group.

A mapping $s : M \rightarrow M$ can be written as

$$s = \left(\begin{array}{c} d_1, d_2, \dots, d_k \\ d_{i_1}, d_{i_2}, \dots, d_{i_1} \end{array} \right). \tag{1}$$

Here we use a product of disjoint cycles as an alternative notation for a mapping [12]. For example,

$$\left(\begin{array}{c} d_1, d_2, d_3, d_4, d_5, d_6, d_7, d_8, d_9 \\ d_1, d_4, d_7, d_2, d_5, d_8, d_3, d_6, d_9 \end{array} \right) \tag{2}$$

can be written as $(d_2, d_4)(d_3, d_7)(d_6, d_8)$. Denote ‘()’ as the identity mappings direct wiring and call this the unity element in a permutation group. The inverse mapping of mapping s is denoted as s^{-1} . As per convention, a product $s \star t$ of two permutations applies mapping s before t .

We order the 3^n different n -input assignment vectors as

$$(0, 0, \dots, 0), (1, 0, \dots, 0), (2, 0, \dots, 0), (0, 1, \dots, 0), \dots, (2, 2, \dots, 2), \tag{3}$$

and denote them by $a_1, a_2, a_3, \dots, a_m$, where $m = 3^n$. Thus a $n \times n$ ternary reversible circuit is just a permutation in S_m (where $m = 3^n$), and vice versa. Cascading two gates is equivalent to multiplying two permutations. In what follows, no distinction between an $n \times n$ reversible gate and a permutation in S_m (where $m = 3^n$) will be made.

Definition 3 (Swap gate). A Swap gate $E_{i,j}$ exchanges the i th bit B_i and the j th bit B_j , i.e. $P_i = B_j, P_j = B_i; P_r = B_r$, if $r \neq i, j$.

Definition 4 (ternary NOT gate). A Ternary NOT Gate N_j is defined as: $P_j = B_j \oplus_3 1$,⁶ $P_i = B_i$, if $i \neq j, 1 \leq j \leq n$.

Definition 5 (ternary Toffoli gate). A Ternary Toffoli Gate T is defined such that if $B_2 = B_3 = \dots = B_n = 1$, then $P_1 = B_1 \oplus_3 1$; otherwise, $P_1 = B_1$, whereas $P_i = B_i$, for $i \neq 1$. In other words, it maps d_1 to d_2, d_2 to d_3, d_3 to d_1 , respectively, where $d_1 = (0, 1, 1, \dots, 1), d_2 = (1, 1, 1, \dots, 1), d_3 = (2, 1, 1, \dots, 1)$, and the other assignment vectors do not change.

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ \dots \end{bmatrix} = \begin{bmatrix} 0, 1, 1, \dots, 1 \\ 1, 1, 1, \dots, 1 \\ 2, 1, 1, \dots, 1 \\ \text{others} \end{bmatrix} \xrightarrow{T} \begin{bmatrix} 1, 1, 1, \dots, 1 \\ 2, 1, 1, \dots, 1 \\ 0, 1, 1, \dots, 1 \\ \text{others} \end{bmatrix} = \begin{bmatrix} d_2 \\ d_3 \\ d_1 \\ \dots \end{bmatrix} \tag{4}$$

From the definition of T , we have $T = (d_1, d_2, d_3)$. Thus, T is a 3-cycle, and $T^{-1} = T \star T, (T \star T)^{-1} = T$.

Definition 6 (j-cycle). Let S_k be a symmetric group of symbols $\{d_1, d_2, \dots, d_k\}$, then $(d_{i_1}, d_{i_2}, \dots, d_{i_j})$, where $j \leq k$, is called a j -cycle. In particular, a j -cycle $(d_i, d_{i+1}, \dots, d_{i+j-1})$ is called a neighbour j -cycle of S_k , for $\forall 1 \leq i \leq k - j + 1$

Definition 7 (even permutation and odd permutation). A permutation is even if it is a product of an even number of 2-cycles and odd if it is a product of an odd number of 2-cycles.

⁶ \oplus_3 denotes addition modulo 3.

Case 1: g is an even reversible circuit. According to lemma 3, g can be generated by some 3-cycle's. According to lemma 4, all 3-cycle's can be generated by Swap, NOT and Toffoli gates. Therefore, g can be generated by Swap, NOT and Toffoli gates.

Case 2: g is an odd reversible circuit. Then $E_{1,2} \star g$ is an even reversible circuit. From case 1, $E_{1,2} \star g$ can be generated by Swap, NOT and Toffoli gates. $(E_{1,2})^{-1} = E_{1,2}$. Thus, g can be generated by Swap, NOT and Toffoli gates. \square

The following algorithm is given to synthesize any $n \times n$ ternary reversible circuit:

Algorithm: Synthesize any $n \times n$ ternary reversible circuit g .

Input: Swap gate, NOT gate, Toffoli gate and g .

- (i) If g is an even permutation,
then $g = C_1 \star C_2 \star \dots \star C_s$; (C_i are 3-cycles for $i = 1, \dots, s$).
- (ii) $C_i = L_{i,1} \star L_{i,2} \star \dots \star L_{i,t_i}$; for $i = 1, 2, \dots, s$. ($L_{i,j}$ are Swap, or NOT, or Toffoli gates).
- (iii) Return $g = [L_{1,1} \star \dots \star L_{1,t_1}] \star \dots \star [L_{s,1} \star \dots \star L_{s,t_s}]$.
- (iv) If g is an odd permutation, then $E_{1,2} \star g = L_1 \star L_2 \star \dots \star L_h$; (where L_i are Swap, or NOT, or Toffoli gates).
- (v) Return $g = E_{1,2} \star L_1 \star \dots \star L_h$.

This algorithm can be implemented in terms of the above lemmas. Line 1 is based on lemma 3. Line 2 is a logical consequence from lemma 4. Line 3 is a direct result from line 1 and 2. In terms of lemma 1 and lines 1, 2, and 3, we have Line 4. From line 4 and lemma 1, line 5 is derived.

In binary reversible logic, there is a result stating that 'All $n \times n$ binary reversible circuits can be generated by Swap, NOT, and Toffoli gates' [15, 17]. This leads to conjecture 1 which represents an open problem. Although it has not been proven yet, we strongly believe that it is true.

Conjecture 1. All $n \times n$ p -value ($p \geq 3$) reversible circuits can be generated by Swap, NOT and Toffoli gates (change modulo 3 to modulo p).

In the following, we give some properties of other ternary gates.

Definition 8 (ternary Controlled-NOT gate). A ternary Controlled-NOT gate $C_{j,i}$ is defined as $P_j = B_j \oplus_3 1$ if $B_i = 1$; otherwise, $P_j = B_j$; further, $P_m = B_m$, if $m \neq j$, Where $1 \leq j \neq i \leq n$.

Definition 9 (ternary Multiply-Two gate). A ternary Multiply-Two gate MT_i is defined as $P_i = B_i \otimes_3 2$; $P_m = B_m$, if $m \neq i$, where \otimes_3 is the operation of multiplication by modulo 3; $1 \leq i \leq n$.

Theorem 2. All $n \times n$ ternary reversible circuits can be generated by NOT, Controlled-NOT, Multiply-Two, and Toffoli gates.

Proof. Using algorithm MLR in [18], we obtain:

$$E_{i,j} = MT_i \star C_{j,i} \star C_{i,j} \star C_{i,j} \star MT_j \star C_{i,j} \star C_{j,i} \star C_{j,i} \star MT_i \star C_{j,i} \star C_{i,j} \star C_{i,j}.$$

From theorem 1, we can draw the conclusion that all $n \times n$ ternary reversible circuits can be generated NOT, Controlled-NOT, Multiply-Two and Toffoli gates. \square

Based on the similarity to binary quantum switching networks, the set of NOT, Controlled-NOT, Multiply-Two and Toffoli gates is a more practical set for synthesis. CNOT is a known gate and widely used gate as is the NOT gate. The Toffoli is a natural extension of CNOT

and NOT gates. Multiply-two is a single qudit gate so it should be not expensive. The cost of quantum gates depends on different technologies. We hope this set has some cost advantage when it is used to realize any ternary reversible circuit. In this paper, we just prove that this set is a universal set. But the synthesis method based on the proof of theorem 2 is not length efficient. We are still looking for a length efficient synthesis algorithm with this set.

3. Conclusion

We demonstrated that ternary Swap, ternary NOT and ternary Toffoli gates are universal for realization of arbitrary ternary $n \times n$ reversible circuits without ancilla bits. We also proved that all $n \times n$ ternary reversible circuits can be generated by NOT, Controlled-NOT, Multiply-Two and Toffoli gates. Our approach is constructive, so it is effective in both space and time resources but not optimal.

The construction of qudit quantum gates (including ternary reversible gates) was discussed in [5–8]. The costs of multi-level reversible gates depend on the realization of technologies. Our next plan is to find the cost of these ternary reversible gates, and create an algorithm with optimal cost by using these gates.

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Appendix. A proof of lemma 4

Lemma 4. For any three different assignment vectors u, s and t , the 3-cycle permutation (u, s, t) can be generated by NOT gate N_j , Swap gate $E_{i,j}$ and Toffoli gate T .

Proof. We denote the vectors u, s and t as the following matrix:

$$P = \begin{bmatrix} u \\ s \\ t \end{bmatrix} = \begin{bmatrix} u_1, u_2, \dots, u_n \\ s_1, s_2, \dots, s_n \\ t_1, t_2, \dots, t_n \end{bmatrix}.$$

In the 3-row matrix P , a column having different elements is called a heterogeneous column. Otherwise, it is called homogeneous column.

Let $H = \begin{bmatrix} P \\ Q \end{bmatrix}$ be the matrix composed of all the 3^n different n -input assignments where Q is composed of $3^n - 3$ different n -input assignment vectors except u, s and t .

From the definition, the operations of Swap, NOT and Toffoli gates on H are as follows.

- Swap gate $E_{i,j}$ interchanges column i and column j .
- NOT gate N_i is an operation $\bigoplus_3 1$ for all elements in column i .
- Toffoli gate T interchanges three rows: $(0, 1, 1, \dots, 1)$ to $(1, 1, 1, \dots, 1)$, $(1, 1, 1, \dots, 1)$ to $(2, 1, 1, \dots, 1)$, $(2, 1, 1, \dots, 1)$ to $(0, 1, 1, \dots, 1)$, and the rest rows remain fixed.

Now we consider the matrix P for the following three cases:

Case 1: There is only one heterogeneous column in the matrix P .

- (i) We can use a Swap gate $E_{i,j}$ to exchange the heterogeneous column to the first column position.
- (ii) Using NOT gates N_j , we can assign all the elements in the homogeneous columns as values 1.

- (iii) Using Toffoli gate T or $T \star T$ gates (if $(u_1, s_1, t_1) = (0, 1, 2)$, or $(1, 2, 0)$, or $(2, 0, 1)$, use T , otherwise $T \star T$), we can reorder the rows r_1, r_2, r_3 to r_2, r_3, r_1 in the matrix P .
- (iv) Finally, using the inverse of the NOT and Swap gates used in steps 2 and 1 to recover the changed digital numbers, we obtain the 3-cycle (u, s, t) .

Denote $P^{(i)}$ and $Q^{(i)}$ as the image matrices of P and Q after the i th step, $i = 1, 2, 3, 4$. Then the operations of the 4th step agree as follows:

$$P^{(3)} \xrightarrow{\text{step 4}} P^{(4)} = \begin{bmatrix} s \\ u \\ t \end{bmatrix}, \quad Q^{(3)} \xrightarrow{\text{step 4}} Q^{(4)} = Q.$$

This process means that an arbitrary 3-cycle permutation (u, s, t) with only one heterogeneous column in the matrix P can be generated by using NOT gates, Swap gates and one or two Toffoli gate(s). Example 1 shows this process.

Example 1. Let $n = 3, u = (0, 0, 2), s = (0, 1, 2), t = (0, 2, 2)$. The column 2 is heterogeneous.

$$\begin{aligned} \begin{bmatrix} u \\ s \\ t \end{bmatrix} &= \begin{bmatrix} 0, 0, 2 \\ 0, 1, 2 \\ 0, 2, 2 \end{bmatrix} \xrightarrow{E_{1,2} \star N_2 \star (N_3)^2} \begin{bmatrix} 0, 1, 1 \\ 1, 1, 1 \\ 2, 1, 1 \end{bmatrix} \xrightarrow{T} \begin{bmatrix} 1, 1, 1 \\ 2, 1, 1 \\ 0, 1, 1 \end{bmatrix} \\ &\xrightarrow{(N_3)^{-2} \star (N_2)^{-1}} \begin{bmatrix} 1, 0, 2 \\ 2, 0, 2 \\ 0, 0, 2 \end{bmatrix} \xrightarrow{(E_{1,2})^{-1}} \begin{bmatrix} 0, 1, 2 \\ 0, 2, 2 \\ 0, 0, 2 \end{bmatrix} = \begin{bmatrix} s \\ t \\ u \end{bmatrix} \end{aligned}$$

Therefore,

$$\begin{aligned} (u, s, t) &= E_{1,2} \star N_2 \star N_3 \star N_3 \star T \star (N_3 \star N_3)^{-1} \star (N_2)^{-1} \star (E_{1,2})^{-1} \\ &= E_{1,2} \star N_2 \star N_3 \star N_3 \star T \star N_3 \star N_2 \star N_2 \star E_{1,2}. \end{aligned}$$

We use notation $(N_3^{-1})(N_3^{-1}) = (N_3)^{-2}$.

In fact, at the end of step 3, we can write a generating expression of (u, s, t) as a product of the Swap gates, NOT gates and Toffoli gates without performing step 4. We perform step 4 in example 1 just to show that this process is correct.

Case 2: There are two heterogeneous columns among u, s and t .

- (i) Using Swap gates, we can exchange columns such that the first and second columns are heterogeneous and the number of different elements in the first column is no more than that in the second column.
- (ii) Using Not gates, set all the elements in the homogeneous columns as values 1.
- (iii) Using Swap, NOT, and Toffoli gates, set the elements of the second columns as value 1.

We have the following three subcases:

- *Subcase 1:* There are two different elements in the first column and three different elements in the second column. Without loss of generality, we assume $u_1 = s_1 \neq t_1$. Consider t_2 . If $t_2 \neq 1$, use N_2 (if $t_2 = 0$) or $N_2 \star N_2$ (if $t_2 = 2$) to interchange t_2 to 1. Then use T (if $t_1 \oplus_3 1 = u_1$) or $T \star T$ (if $t_1 \oplus_3 2 = u_1$) to interchange t_1 to u_1 . If $u_1 = s_1 = t_1 \neq 1$, use N_1 or $N_1 \star N_1$ to make the elements in column 1 be 1s. Finally, exchange columns 1 and 2. As a result, the elements in the first column are different and the elements of other elements in P are all 1s.
- *Subcase 2:* There are two different elements in the first column and the second column, respectively. Without loss of generality, we assume $u_2 = s_2 \neq t_2$. Then $u_1 \neq s_1$. We

use NOT gate(s) to change u_2 and s_2 to 1 s if they are NOT 1s. Then use T or $T \star T$ to change u_1 and s_1 such that the elements in the first column are different with each other. Finally, exchange columns 1 and 2. Then, the resulting matrix P becomes the subcase 1.

- *Subcase 3:* There are three different elements in the first column and the second column, respectively. Without loss of generality, we assume $u_2 = 1$. After using T , we change u_1 to s_1 or t_1 . Then, the resulting matrix P becomes the subcase 1. For instance,

$$\begin{bmatrix} u \\ s \\ t \end{bmatrix} = \begin{bmatrix} 0, 2, 1 \\ 1, 0, 1 \\ 2, 1, 1 \end{bmatrix} \xrightarrow{T} \begin{bmatrix} 0, 2, 1 \\ 1, 0, 1 \\ 0, 1, 1 \end{bmatrix} \text{ (This is subcase 1).}$$

- (iv) Using Toffoli gate T or $T \star T$ to change the order of the first three vectors as expected (we can reorder the rows r_1, r_2, r_3 to r_2, r_3, r_1).
- (v) Finally, using the inverse of these NOT gates, Swap gates and Toffoli gates in the steps 3, 2, and 1 to recover these changed digital numbers, we obtain the 3-cycle (u, s, t) .

The action of the 5th step is:

$$P^{(4)} \xrightarrow{\text{step 5}} P^{(5)} = \begin{bmatrix} s \\ t \\ u \end{bmatrix}, \quad Q^{(4)} \xrightarrow{\text{step 5}} Q^{(5)} = Q.$$

Example 2 shows the process executed in case 2.

Example 2. Let $n = 3, u = (0, 0, 1), s = (0, 0, 2), t = (1, 0, 1)$.

$$\begin{aligned} \begin{bmatrix} u \\ s \\ t \end{bmatrix} &= \begin{bmatrix} 0, 0, 1 \\ 0, 0, 2 \\ 1, 0, 1 \end{bmatrix} \xrightarrow{E_{2,3}} \begin{bmatrix} 0, 1, 0 \\ 0, 2, 0 \\ 1, 1, 0 \end{bmatrix} \xrightarrow{N_3} \begin{bmatrix} 0, 1, 1 \\ 0, 2, 1 \\ 1, 1, 1 \end{bmatrix} \text{ (Step 1 and; 2)} \\ &\xrightarrow{T} \begin{bmatrix} 1, 1, 1 \\ 0, 2, 1 \\ 2, 1, 1 \end{bmatrix} \xrightarrow{E_{1,2}} \begin{bmatrix} 1, 1, 1 \\ 2, 0, 1 \\ 1, 2, 1 \end{bmatrix} \left(\begin{array}{l} \text{Now it} \\ \text{becomes} \\ \text{subcase 1} \end{array} \right) \text{ (End step 3)} \\ &\xrightarrow{T \star T} \begin{bmatrix} 1, 1, 1 \\ 0, 1, 1 \\ 2, 1, 1 \end{bmatrix} \text{ (End step 4)} \xrightarrow{(E_{1,2}^{-1}) \star (T \star T)^{-1} \star (N_2)^{-1}} \begin{bmatrix} 2, 0, 1 \\ 1, 2, 1 \\ 1, 1, 1 \end{bmatrix} \\ &\xrightarrow{(E_{1,2})^{-1} \star T^{-1}} \begin{bmatrix} 0, 2, 1 \\ 1, 1, 1 \\ 0, 1, 1 \end{bmatrix} \xrightarrow{(N_3)^{-1} \star (E_{2,3})^{-1}} \begin{bmatrix} 0, 0, 2 \\ 1, 0, 1 \\ 0, 0, 1 \end{bmatrix} = \begin{bmatrix} s \\ t \\ u \end{bmatrix} \end{aligned}$$

Therefore,

$$\begin{aligned} (u, s, t) &= E_{2,3} \star N_3 \star T \star E_{1,2} \star N_2 \star T \star T \star E_{1,2} \star (T \star T) \star (E_{1,2})^{-1} \\ &\quad \star (T \star T)^{-1} \star (N_2)^{-1} \star (E_{1,2})^{-1} \star (T)^{-1} \star (N_3)^{-1} \star (E_{2,3})^{-1} \\ &= E_{2,3} \star N_3 \star T \star E_{1,2} \star N_2 \star T \star T \star E_{1,2} \star (T \star T) \star E_{1,2} \\ &\quad \star T \star N_2 \star N_2 \star E_{1,2} \star T \star T \star N_3 \star N_3 \star E_{2,3}. \end{aligned}$$

In fact, after step 4, we can write a generating expression of (u, s, t) as a product of the Swap gates, NOT gates, and Toffoli gates without executing step 5. We perform step 5 in Example 2 just to show that the process is correct.

Note: After finishing the whole process in case 1 and 2, the remaining $27 - 3 = 24$ rows are not affected by the string of gates. And in the process, we can find the realization without considering these 24 rows. Thus, we only act these gates on the three rows u , s and t .

Case 3: There are more than two different bits among u , s and t .

Similar to the binary reflective Gray code [19], we can also reflectively encode the ternary vectors in an order x_1, x_2, \dots, x_m , where $m = 3^n$ such that there is only one bit different between the two vectors x_i and x_{i+1} , for $1 \leq i \leq m - 1$. Therefore, we can find $i < j < k$, such that x_i, x_j , and x_k are a permutation of u, s , and t , respectively. Namely, $(u, s, t) = (x_i, x_j, x_k)$ or $(u, s, t) = (x_i, x_j, x_k)^2$.

There are at most two different bits among x_h, x_{h+1}, x_{h+2} , for $1 \leq h \leq m - 2$. According to case 1 and case 2, the 3-cycle (x_h, x_{h+1}, x_{h+2}) can be generated by Swap, NOT and Toffoli gates. Thus, according to lemma 3, the 3-cycle (x_i, x_j, x_k) can be generated by Swap, NOT and Toffoli gates. As a result, (u, s, t) can be generated by Swap, NOT and Toffoli gates.

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